APPLICATION
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Title: **INTEGRATED CIRCUIT REDISTRIBUTION PACKAGE**

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Application Of: Timothy W. Budell, Eric W. Tremble and Brian P. Welch

For: INTEGRATED CIRCUIT REDISTRIBUTION PACKAGE

Background Of The Invention

1. Field of the Invention

[0001] This invention relates to the field of integrated circuit chip packaging, and more specifically to devices for connecting an integrated circuit chip to a printed circuit board. **2. Description of Prior Art**

[0002] Integrated circuit chips have a large number of pins that must be connected to a circuit board. The circuit board sends and receives signals from the integrated circuit chip and also provides power and ground for the chip. Integrated circuit chips are small in comparison to circuit boards and typically have pins that are separated by 100μm to 200μm. The circuit boards to which integrated circuit chips are connected have connector pads that typically are separated by no less than approximately 1 mm.

[0003] It is necessary to provide means for connecting the closely-spaced contacts of integrated circuit chips to the more widely-spaced contacts of a circuit board. The connections between the chip and the printed circuit board include ground, power and signal. To maintain separation between signal paths, typical architecture requires one or more signal layers, separated from each other by one or more power planes or ground planes to reduce signal interference. Signal, ground and power layers are electrically isolated from each other by interposed layers of dielectric. Typical redistribution packages comprise closely-spaced contacts that match the contacts of an integrated circuit chip and communicate electrically with the traces on the otherwise isolated signal layers, ground layers and power layers by vias.

The traces on different signal, ground and power layers are connected to traces on respective other signal, ground and power layers through the use of vias that provide electrical communication between otherwise isolated layers. The signal, ground and power layers are also connected by vias to more widely-spaced contacts of the redistribution package that communicate with contacts on the circuit board.

[0004] Signal vias, however, can generate "cavity noise" that results from the interruption of displacement current whenever switching activity occurs thereon. In addition, these prior art coplanar redistribution packages often suffer from signal noise due to signal coupling.

3. Objects and Advantages

[0005] It is therefore a principal object and advantage of the present invention to provide a redistribution package that permits connection of a chip to a printed circuit board without generating cavity noise.

[0006] It is an additional object and advantage of the present invention to provide a redistribution package that does not utilize signal vias.

[0007] It is a further object and advantage of the present invention to provide a redistribution package that diminishes the likelihood of noise coupling in the package.

[0008] Other objects and advantages of the present invention will in part be obvious, and in part appear hereinafter.

Summary of the Invention

[0009] In accordance with the foregoing objects and advantages, the present invention provides a redistribution package having an upper surface that includes contacts with reduced pitch that corresponds, for example, to that of a Controlled Collapse Chip Connection ("C4") structure formed on a chip, and a lower surface having contacts with increased pitch that correspond, for example, to a printed circuit

board employing ball grid array ("BGA") pads. A series of power, signal and ground conductors extend through the body of the redistribution package and interconnect the circuit board contacts to the chip contacts.

[0010] In one aspect, the redistribution package of the present invention comprises a truncated pyramidal shaped body having four sloping, lateral sides extending between planar upper and lower contact surfaces. The upper surface, preferably rectangular in form, is parallel to and proportionately smaller than the bottom surface, which is also preferably rectangular in form. Conductors extending through the body at a plurality of angles interconnect the contacts on the top surface to the contacts on the bottom surface. A chip having contacts that are arranged in the same pattern as the contacts on the upper surface is electrically connected to the upper surface, while an integrated circuit board having contacts arranged in the same pattern as the contacts on the lower surface of the redistribution package is electrically connected to the lower surface. Signal carrying conductors, ground conductors, and power conductors extend through the body at a plurality of angles and interconnect respective pairs of lower surface contacts with upper surface contacts. Each signal carrying conductor is surrounded on all four sides by ground conductors to eliminate signal coupling and cavity noise.

[0011] In another aspect of the invention, the structure of the redistribution package is modified to include a power plane that is coextensive with and parallel to the upper surface of the redistribution package. A plurality of power conductors extend through the redistribution package to carry power from the integrated circuit board to the power plane and ultimately to the chip. A plurality of vias are formed through the power plane and provide electrically isolated passageways for the ground

and signal carrying conductors which extend between the upper and lower surfaces of the redistribution package.

Brief Description Of The Drawings

[0012] The present invention will be more fully understood and appreciated by reading the following Detailed Description in conjunction with the accompanying drawings, in which:

[0013] Fig. 1 is a top plan view of an integrated circuit chip mounted to a circuit board using the present invention;

[0014] Fig. 2 is a perspective view of a redistribution package according to the present invention;

[0015] Fig. 3 is a perspective view of an integrated circuit chip for use with the present invention;

[0016] Fig. 4 is a perspective view of a circuit board for use with the present invention;

[0017] Fig. 5 is a side elevation view of an integrated circuit chip mounted to a circuit board using the present invention;

[0018] Fig. 6 is a side elevation view taken in section of a redistribution package according to the present invention;

[0019] Fig. 7 is a top plan view of a redistribution package according to one embodiment of the present invention;

[0020] Fig. 8 is a partial, perspective view taken in section of a redistribution package according to a second embodiment of the present invention;

[0021] Fig. 9 is a top plan view of a redistribution package according to a third embodiment of the present invention; and

[0022] Fig. 10 is a partial side elevation view taken in section of an integrated

circuit chip mounted to a circuit board using a fourth embodiment of the present invention.

Detailed Description

[0023] Referring now to the drawings, wherein like reference numerals refer to like parts throughout, there is seen in Figure 1 a redistribution package, designated generally by reference numeral 10, for electrically interconnecting an integrated circuit chip 12 to an integrated circuit board 14. Chip 12 is any type of chip that is generally used in the electronics industry and includes a plurality of electrical contacts 16 (see Fig. 3) disposed on its bottom surface, such as for example, C4 connections. Board 14 is a typical integrated circuit board and is provided with a plurality of electrical contacts 18 (see Fig. 4) in a predetermined format, such as in a ball grid array (BGA). As is typical, contacts 16 are arranged in a much finer pitch pattern than are contacts 18. For example, contacts 16 may be spaced apart by about 100 μm – 200 μm, while contacts 18 may be spaced no less than approximately 1 mm apart. Redistribution package 10 provides effective electrical interconnection between respective pairs of contacts 16 and 18.

[0024] With reference to Figs. 1-5, redistribution package 10 generally comprises a truncated pyramidal shaped body defined by an upper surface 20 with a plurality of contacts 22 disposed thereon, a lower surface 24 with a plurality of contacts 26 (see Fig. 6) disposed thereon, and sidewalls 28 that slope inwardly from bottom surface 24 to upper surface 20. In its preferred embodiment, upper surface 20 and lower surface 24 have generally rectangular peripheral edges and extend in planes that are held in spaced, parallel relation to one another by sidewalls 28.

[0025] In order to provide effective and accurate electrical conductance between contacts 18 and contacts 16, contacts 22 formed on upper surface 20 are

arranged in essentially the same manner as contacts 16, while contacts 26 formed on lower surface 24 are arranged in essentially the same manner as contacts 26. In order to electrically interconnect respective pairs of contacts 22 and 26, a plurality of conductors 30 extend through package 10, as seen in Fig. 5. Due to the shape of package 10, i.e., pyramidal, conductors 30 extend at various oblique angles between respective pairs of contacts 22 and 26 for reasons that will be more fully explained hereinafter.

[0026] With reference to Fig. 6, to maintain signal integrity and prevent unwanted noise, conductors 30 are separated from one another by dielectric material 32. Each conductor 30 electrically interconnects one of contacts 22 to a corresponding one of contacts 26; that is, a contact 22 in the first row and first column of the grid of contacts 22 will be interconnected to a contact 26 that is in the first row and first column of the grid of contacts 26.

[0027] The pyramidal shape of package 10 permits conductors 30 to extend in two dimensions along essentially straight paths (i.e., the conductors extend along an inclined path or slope). The degree of inclination of a conductor 30 will vary depending on its proximity to the center of package 10. For instance, a conductor 30 that is near the edge of package 10 (i.e., a conductor interconnecting contacts 22 and 26 that are at or near the edge of upper and lower surfaces 20 and 24, respectively) will have a less vertical angular inclination than will a conductor that is positioned more towards the center of package 10 (at the geometric center of package 10, the conductor would essentially be vertical).

[0028] Conductors 30 may be either signal carrying conductors 30a, ground conductors 30b, or power conductors 30c (see Figs. 6, 7), that provide signal, ground and power connections between contacts 22 and 26, respectively. It is advantageous

to arrange the signal 30a, ground 30b and power 30c conductors in a manner that minimizes noise and interference.

[0029] In one embodiment, as seen in Figure 7, a plurality of concentric rings of conductors 30 are arranged, with each ring comprising entirely signal conductors 30a, ground conductors 30b, or power conductors 30c. For example, the outermost concentric ring might comprise ground conductors 30b with the next inner ring comprising signal conductors 30a, and the next inner ring comprising power conductors 30c. Other concentric rings formed in package 10 are comprised entirely of one type of conductor 30 (i.e., signal conductors 30a, ground conductors 30b, or power conductors 30c), and may alternate in any order. It is advantageous for signal integrity that each ring of signal conductors 30a be positioned between a ring of ground conductors 30b and a ring of power conductors 30c.

[0030] In another embodiment, each signal conductor 30a is surrounded on all four sides by a ground conductor 30b, as illustrated in Figs. 8 - 9 (referred to as microstrip architecture or straight line redistribution), with the conductors being aligned along planes defined by axes A-A and B-B. To maintain a constant impedance along the length of signal conductors 30a, and due to the angle of inclination at which the conductors extend, the cross-sectional dimensions of the ground conductors 30b must increase from upper surface 20 (represented by t1) towards lower surface 24 (represented by t2) to maintain a constant distance from adjacent signal conductors 30a, as seen in Fig. 6. Maximum utilization of signal wiring channels in this embodiment may be achieved by positioning signal conductors 30a in the outermost concentric ring and surrounding each signal conductor 30a on three sides by ground conductors 30b. According to this embodiment, power may be supplied to chip 12 by a concentric ring of power conductors 30c, or by at least one

power conductor 30c positioned within the grid of conductors 30.

[0031] In a further embodiment of the present invention, as shown in Fig. 10, power is distributed to chip 12 by means of at least one power layer 34. Each power layer 34 is in a plane that is essentially parallel to and coextensive with upper surface 20. Each power layer 34 is comprised of at least one power reference metal 42. Power is provided to power layer 34 by at least one power conductor 30c positioned within the conductor grid, or by a separate power structure. If there is more than one power layer 34, power is transmitted between them by means of power vias 36 that interconnect like power reference metals 42 on the various power layers. Power layer 34 is isolated from signal conductors 30a and ground conductors 30b by one or more layers of dielectric material 38. According to this embodiment, upper contacts 22 are connected to signal conductors 30a and ground conductors 30b by vias 40 that extend through and are isolated from power layer 34.

[0032] Integrated circuit chips may require power to be provided in a plurality of voltages. In the preferred embodiment, a plurality of voltages can be supplied to an integrated circuit chip through redistribution package 10 by providing at least one distinct power conductor 30c for each distinct voltage that is required for operation of the integrated circuit chip. In an alternate embodiment of redistribution package 10 that contains a power layer 34, a plurality of voltages can be supplied to an integrated circuit chip through redistribution package 10 by providing at least one distinct power conductor 30c and at least one distinct power reference metal 42 for each distinct voltage required for operation of the integrated circuit chip.

[0033] While there has been illustrated and described what are at present considered to be preferred and alternate embodiments of the present invention, it

should be understood and appreciated that modifications may be made by those skilled in the art, and that the appended claims encompass all such modifications that fall within the full spirit and scope of the present invention.